WHAT IS CLAIMED IS:

1   1.   A data processor comprising:

2   an instruction execution pipeline comprising N processing

3   stages capable of executing a load instruction;

4   a status register capable of storing a modifiable

5   configuration value, said modifiable configuration value having a

6   first value indicating said data processor is capable of executing

7   a misaligned access handling routine and a second value indicating

8   said data processor is not capable of executing a misaligned access

9   handling routine;

10   a misalignment detection circuit capable of determining

11   if said load instruction performs a misaligned access to a target

12   address of said load instruction and, in response to a

13   determination that said load instruction does perform a misaligned

14   access, generating a misalignment flag; and

15   exception control circuitry capable of detecting said

16   misalignment flag and in response thereto determining if said

17   modifiable configuration value is equal to said first value.

1   2.   The data processor as set forth in Claim 1 wherein said

2   exception control circuitry, in response to a determination that

3   said modifiable configuration value is equal to said first value,

4   causes said data processor to execute said misaligned access

5   handling routine.

1   3.   The data processor as set forth in Claim 2 wherein said

2   exception control circuitry, in response to a determination that

3   said modifiable configuration value is equal to said second value,

4   determines if said load instruction is speculative.

1   4.   The data processor as set forth in Claim 3 wherein said

2   exception control circuitry, in response to a determination that

3   said load instruction is speculative, causes said data processor to

4   dismiss said load instruction.

1   5.   The data processor as set forth in Claim 4 further

2   comprising a data protection unit capable of determining if said

3   load instruction accesses a restricted area of memory.

1   6.   The data processor as set forth in Claim 5 wherein said

2   data protection unit, in response to a determination that said load

3   instruction does access a restricted area of memory, causes said

4   data processor to execute an exception handling routine.

1   7.   The data processor as set forth in Claim 6 wherein said

2   data protection unit, in response to a determination that said load

3   instruction does access a restricted area of memory, is further

4   capable of determining if said load instruction is speculative.

1   8.   The data processor as set forth in Claim 7 wherein said

2   exception control circuitry, in response to a determination that

3   said load instruction is speculative, causes said data processor to

4   dismiss said load instruction.

1   9.   A processing system comprising:

2   a data processor;

3   a memory coupled to said data processor;

4   a plurality of memory-mapped peripheral circuits coupled

5 to said data processor for performing selected functions in

6 association with said data processor, said data processor

7 comprising:

8   an instruction execution pipeline comprising N

9 processing stages capable of executing a load instruction;

10   a status register capable of storing a modifiable

11 configuration value, said modifiable configuration value

12 having a first value indicating said data processor is capable

13 of executing a misaligned access handling routine and a second

14 value indicating said data processor is not capable of

15 executing a misaligned access handling routine;

16   a misalignment detection circuit capable of

17 determining if said load instruction performs a misaligned

18 access to a target address of said load instruction and, in

19 response to a determination that said load instruction does

20 perform a misaligned access, generating a misalignment flag;

21 and

22   exception control circuitry capable of detecting

23   said misalignment flag and in response thereto determining if

24   said modifiable configuration value is equal to said first

25   value.

1   10. The processing system as set forth in Claim 9 wherein

2   said exception control circuitry, in response to a determination

3   that said modifiable configuration value is equal to said first

4   value, causes said data processor to execute said misaligned access

5   handling routine.

1   11. The processing system as set forth in Claim 10 wherein

2   said exception control circuitry, in response to a determination

3   that said modifiable configuration value is equal to said second

4   value, determines if said load instruction is speculative.

1   12. The processing system as set forth in Claim 11 wherein

2   said exception control circuitry, in response to a determination

3   that said load instruction is speculative, causes said data

4   processor to dismiss said load instruction.

1   13.   The processing system as set forth in Claim 12 further

2   comprising a data protection unit capable of determining if said

3   load instruction accesses a restricted area of memory.

1   14.   The processing system as set forth in Claim 13 wherein

2   said data protection unit, in response to a determination that said

3   load instruction does access a restricted area of memory, causes

4   said data processor to execute an exception handling routine.

1   15.   The processing system as set forth in Claim 14 wherein

2   said data protection unit, in response to a determination that said

3   load instruction does access a restricted area of memory, is

4   further capable of determining if said load instruction is

5   speculative.

1   16.   The processing system as set forth in Claim 15 wherein

2   said exception control circuitry, in response to a determination

3   that said load instruction is speculative, causes said data

4   processor to dismiss said load instruction.

1   17.   For use in a data processor comprising: 1) an instruction

2   execution pipeline comprising N processing stages capable of

3   executing a load instruction and 2) a status register capable of

4   storing   a   modifiable   configuration   value,   the   modifiable

5   configuration value having a first value indicating the data

6   processor is capable of executing a misaligned access handling

7   routine and a second value indicating the data processor is not

8   capable of executing a misaligned access handling routine, a method

9   of handling exceptions in the data processor comprising the steps

10   of:

11   determining if the load instruction is performing a

12   misaligned access to a target address of the load instruction;

13   in response to a determination that the load instruction

14   is performing a misaligned access, generating a misalignment flag;

15   detecting the misalignment flag and in response thereto

16   determining if the modifiable configuration value is equal to the

17   first value.

1   18.   The method as set forth in Claim 17 further comprising

2   the step of:

3   in response to a determination that the modifiable

4   configuration value is equal to the first value, executing the

5   misaligned access handling routine.

1   19.   The method as set forth in Claim 18 further comprising

2   the step of:

3   in response to a determination that the modifiable

4   configuration value is equal to the second value, determining if

5   the load instruction is speculative.

1   20.   The method as set forth in Claim 19 further comprising

2   the step of:

3   In response to a determination that the load instruction

4   is speculative, causing the data processor to dismiss the load

5   instruction.